WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells arranged in rows and columns and a plurality of spare memory cells arranged so as to form first and second spare rows in respective regions adjacent to said plurality of memory cells;

a plurality of word lines provided correspondingly to respective rows of said plurality of memory cells;

first and second spare word lines provided correspondingly to said first and second spare rows, respectively;

a plurality of word line drivers provided correspondingly to said respective plurality of word lines to each control a voltage on a corresponding one of said plurality of word lines; and

first and second spare word line drivers provided correspondingly to said first and second spare word lines, respectively, to control voltages on said first and second spare word lines, wherein

said plurality of word line drivers and said first and second spare word line drivers are sequentially disposed in accordance with arrangement of said plurality of word lines and said first and second spare word lines in said memory cell array,

each of said plurality of word line drivers and said first and second spare word line drivers includes:

an output node;

a drive circuit driving a corresponding one of said plurality of word lines and said first and second spare word lines into one of a selected state and a non-selected state according to a voltage at said output node; and

a precharge switch precharging said output node to a first voltage prior to a row select operation and, also, disconnecting said output node from said first voltage in said row select operation,

each of said plurality of word line drivers further includes:

a decode unit connecting a first internal node to a second voltage in said row select operation according to a result of row selection;

a control switch provided between a second internal node and said first internal node to connect both to each other in said row select operation and, also, disconnect both from each other prior to said row select operation;

a first shift switch connected between one output node adjacent to said output node of a corresponding one of said plurality of word line drivers on a first side along a direction of arrangement of said plurality of word line drivers and said first and second spare word line drivers, and said second internal node of said corresponding one of said plurality of word line drivers;

a second shift switch connected between said output node of said corresponding one of said plurality of word line drivers, and said second internal node of said corresponding one of said plurality of word line drivers; and

a third shift switch connected between one output node adjacent to said output node of said corresponding one of said plurality of word line drivers on a second side opposite to said first side, and said second internal node of said corresponding one of said plurality of word line drivers, and

said semiconductor memory device further comprises a shift control circuit controlling turning-on and -off of said first to third shift switches in each of said plurality of word line drivers in said row selection operation on the basis of an address of a defective memory cell row.

2. The semiconductor memory device according to claim 1, wherein

when a defective memory cell row is present, said shift control circuit controls turning-on and -off of said first to third shift switches in each of said plurality of word line drivers so that said output node of the word line driver for a defective word line corresponding to said defective memory cell row is disconnected from said second internal node of any of said plurality of word line drivers, and said output node of at least one of said first and second spare word lines and the output nodes corresponding to the other respective word lines except for said defective word line are connected to respective second internal nodes of said plurality of word line drivers.

3. The semiconductor memory device according to claim 1, wherein said drive circuit drives the corresponding one of said plurality of word lines and said first and second spare word lines into said non-selected state when the corresponding output node is at said first voltage and, also, drives said corresponding one word line into said selected state when said corresponding output node is at said second voltage.

4. The semiconductor memory device according to claim 1, wherein said decode switch connects said first internal output node and said second voltage in one of said plurality of word line drivers according to said result of row selection and, also, disconnects said first internal node from said second voltage in each of the other word line drivers.

5. A semiconductor memory device comprising:

a memory cell array including a plurality of memory cells arranged in rows and columns and a plurality of spare memory cells arranged so as to form J spare rows (where J is a natural number);

a plurality of word lines provided correspondingly to respective rows of said plurality of memory cells;

J spare word lines provided correspondingly to said respective J spare rows;

a plurality of word line drivers provided correspondingly to said respective plurality of word lines to each control a voltage on a corresponding one of said plurality of word lines; and

J spare word line drivers provided correspondingly to said respective J spare word lines to each control a voltage on a corresponding one of said J spare word lines, wherein

said plurality of word line drivers and said J spare word line drivers are sequentially arranged in accordance with arrangement of said plurality of word lines and said J spare word lines in said memory cell array,

each of said plurality of word line drivers and said J spare word line drivers includes:

an output node;

a drive circuit driving a corresponding word line or a spare word line into one of a selected state and a non-selected state according to a voltage at said output node; and

a precharge switch precharging said output node to a first voltage prior to a row select operation and, also, disconnecting said output node from said first voltage in said row select operation,

each of said plurality of word line drivers further includes:

a decode switch connecting a first internal node to a second voltage according to a result of row selection;

a control switch provided between said first internal node and a second internal node to connect both to each other in said row select operation and, also, disconnect both from each other prior to said row select operation; and

(J + 1) shift switches, respectively, provided between said output node of a corresponding one of said plurality of word line drivers and output nodes of adjacent J ones among the other word line drivers and said J spare word line drivers, and said second internal node of said corresponding one of said plurality of word line drivers, and, in said row select operation, one of which is selectively turned on, while the other of which are turned off, and

said semiconductor memory device further comprises a shift control circuit controlling turning-on and -off of said (J + 1) shift switches in each of said plurality of word line drivers in said row selection operation on the basis of an address of a defective memory cell row.

6. The semiconductor memory device according to claim 5, wherein

when said defective memory cell row is present, said shift control circuit controls turning-on and -off of said (J+1) shift switches in each of said plurality of word line drivers so that said output node of the word line driver for a defective word line corresponding to said defective memory cell is disconnected from said second internal node of any of said plurality of word line drivers, and said output node of at least one of said J spare word lines and the output nodes corresponding to the other respective word lines

except for said defective word line are connected to respective second internal nodes of said plurality of word line drivers.

7. The semiconductor memory device according to claim 5, wherein said drive circuit drives the corresponding one of said plurality of word lines or the corresponding one of said J spare word lines into said non-selected state when said corresponding output node is at said first voltage and, also, drives said corresponding one word line or said corresponding one of J spare word lines into said selected state when said corresponding output node is at said second voltage.

8. The semiconductor memory device according to claim 5, wherein said decode switch connects said first internal output node and said second voltage to each other in one of said plurality of word line drivers according to said result of row selection and, also, disconnects said first internal node from said second voltage in each of the other word line drivers.